PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1449	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	200208752-1	10/614,309	
	APPLICANT: Benjamin J. Patella, et al.		
(Use several sheets if necessary)	FILING DATE	GROUP: 2816	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
M	1A	2002/0130095	09-19-2002	Jesephson et al.	713/400
M	1B	6,509,788	01-21-2003	Naffziger et al.	327/548
M	1C	6,489,834	12-03-2002	Naffziger et al.	327/534
	1D				
	1E	6,804,793			
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

M	1Q	Dhar, S., et al., "Low-Power Digital Filtering Using Multiple Voltage Distribution and Adaptive Voltage Scaling," International Symposium on Low Power Electronic Design, (2000), pp. 207-209.
M	1R	Chandrakasan, A., et al., "Design of High-Performance Microprocessor Circuits," IEEE Press, (2001), pp. 120, 128. a pages
M	1S	Kuroda, T., et al., "Variable Supply-Voltage Scheme for Low-Power High Speed CMOS Digital Design," IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, (March 1998), pp. 454-462.

EXAMINER	DATE CONSIDERED
[signature]	3/31/05

Rev 05/03 (PTO1449)